SMQ-080/P6300

United States Application

Entitled: A TWO-PIN THERMAL SENSOR CALIBRATION INTERFACE

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A TWO-PIN THERMAL SENSOR CALIBRATION INTERFACE

Technical Field of the Invention

The present invention generally relates to an integrated circuit, and more particularly, to a sensor circuit having a serial interface.

Background of the Invention

Temperature gradients across the die of today's high performance very large scale integration (VLSI) components, such as a microprocessor can adversely affect component performance. For example, a temperature variation between two clock driver circuits within a microprocessor often results in system clock skew. Moreover, the die may reach an unacceptable temperature that causes the microprocessor to malfunction or stop functioning.

To protect the microprocessor from thermal damage, a diode is typically placed in the die of the microprocessor to provide a die temperature indication. This diode is driven with a fixed amount of current, and the corresponding voltage drop across the diode provides an indication of the microprocessor temperature. Unfortunately, the diode gives no indication that the diode is operating properly. Moreover, the diode has poor accuracy. The diode provides a temperature reading that is accurate to about ±10°C.

Because there is only a single diode positioned at a single location on the microprocessor die to measure the temperature of the microprocessor, it is difficult to

determine the temperature gradient across the microprocessor. Consequently, early indications that a thermal related problem exists in a portion of the microprocessor are difficult to detect. Moreover, given the need to keep microprocessor pinout density to a minimum along with the surface area of the microprocessor, the use of multiple temperature sensors having interfaces external to the microprocessor is prohibitive.

Summary of the Invention

The present invention addresses the above-described limitations of measuring the temperature of an integrated circuit. The present invention provides an approach to enable a sensor of any type to report a sensed value and to indicate a state of operability via an off chip interface having a minimum number of electrical contacts.

In one embodiment of the present invention, a sensor having a register to hold a response to a sensed physical stimulus and an interface to communicate the response is provided. The sensor communicates the response from the register in a manner that indicates whether the sensor is functioning correctly. The interface is a digital interface having at least two electrical contacts. The first contact receives a trigger to initiate the sense operation and the second electrical contact communicates the sensor response. The sensor communicates its response directly to an apparatus or another integrated circuit, or to another circuit within the integrated circuit the sensor is part of. The sensor provides an absolute or relative value of the sensed physical stimulus. In addition, the sensor communicates via the interface to indicate when the sensor is sensing a physical stimulus.

The above-described approach benefits an integrated circuit that seeks a sensor capable of indicating its operability while keeping the external pin density of the integrated circuit to a minimum. As a result, an integrated circuit can communicate an accurate internal temperature reading from an internal sensor to a device external to the integrated circuit and provide an indication of the sensor's operability as part of the communication without significantly increasing external pin density of the packaged integrated circuit.

In accordance with another aspect of the present invention, a method is performed in a sensor that indicates a sensor status, a response of the sensor and the sensor's operational state. By triggering the sensor to sense a physical stimulus, the sensor reports an indication that a sensing operation is in process, a response to the physical stimulus along with a value that is indicative of the sensor's operational state. The response provided by the sensor has a first portion that is indicative of an absolute or relative value of the sensed physical stimulus and a second portion that is indicative of the operational state of the sensor itself.

The above-described approach benefits a microprocessor architecture that utilizes an active sensor. Because the sensor reports a value indicative of its operational state the microprocessor architecture can be assured that the sensor is operating properly. As a result, the reliability and the confidence of the sensor's response is significantly increased.

In yet another aspect of the present invention, a sensor that reports a response value and a status value when triggered is provided. The sensor includes a serial

interface having one input contact and one output contact. The sensor can be a thermal sensor that reports an absolute or relative temperature value.

In still another aspect of the present invention, a method is performed in a very large scale integration (VLSI) circuit for reporting a temperature sensed by a thermal sensor of the VLSI circuit. By triggering the thermal sensor to sense the temperature of the VLSI circuit the thermal sensor senses the die or package temperature of the VLSI circuit and affixes a value to the sensed temperature that indicates whether the sensor is functioning properly. The thermal sensor reports the sensed temperature value with the affixed value to a device either internal to or external to the VLSI circuit. From the affixed value, the receiving device can determine whether the temperature value provided is reliable or unreliable. Moreover, the thermal sensor of the VLSI circuit can sense and report a temperature of the system in which the VLSI circuit operates.

Brief Description of the Drawings

An illustrative embodiment of the present invention will be described below relative to the following drawings.

Figure 1 depicts a block diagram of an integrated circuit suitable for practicing the illustrative embodiment of the present invention.

Figure 2 illustrates a timing diagram suitable for practicing the illustrative embodiment of the invention.

Figure 3 is a flow diagram that depicts operation of the illustrative embodiment of the invention.

Detailed Description

The illustrative embodiment of the present invention provides a sensor that indicates whether it is functioning properly, whether it is sensing or not and a response to a physical stimulus. In the illustrative embodiment a sensor is adapted to have a serial interface to report three data values in response to a control signal that initiates a sensing process. A first data value indicates whether a sensing operation is in process, a second value represents a response to the sensed physical stimulus and a third data value indicates whether the sensor is functioning properly.

In the illustrative embodiment, the sensor is attractive for use in integrated circuits that need to keep external pins to a minimum while accurately tracking the temperature of the integrated circuit itself. The sensor allows an integrated circuit, such as a microprocessor, to communicate an accurate temperature value of the circuit in a reliable manner. The illustrative embodiment allows for an active device to be used to sense and report a temperature value along with an indication of the sensor's operability without significantly impacting the surface area or the pinout density of the integrated circuit.

Figure 1 is a block diagram of an exemplary integrated circuit 12 that is suitable for practicing the illustrative embodiment of the present invention. The

sensor 14 is an active device within the exemplary integrated circuit 12. The sensor 14 includes a register to hold a response to a physical stimulus. Coupled to the sensor 14 are the clock input node 24, the power input node 22, the ground node 20, the input node 18 and the output node 16. Input node 18 and output node 16 provide the sensor 14 with an interface external to the exemplary integrated circuit 12. The power input node 22 is tied to a voltage source that can be controlled independently of the voltage source supplying a voltage level to the remainder of the active devices within the exemplary integrated circuit 12. The clock node 24 is also coupled to a clock source or driver that can be controlled independently of any other clock source driver within the exemplary integrated circuit 12. As a consequence, the sensor 14 can be operated independently of the exemplary integrated circuit 12 and therefore used to determine a base line temperature of the exemplary integrated circuit 12 for calibration purposes. In this manner, the sensor 14 can be calibrated without having to compensate for the thermal affects of having one or more other active elements within the exemplary integrated circuit 12 active during baselining.

The input node 18 is adapted to receive a digital input signal that triggers the sensor 14 to sense a physical stimulus and report a response corresponding to an absolute or relative value of the physical stimulus. The output node 16 is adapted to communicate a digital signal that indicates that the sensor 14 is in process of sensing a physical stimulus, the response held by the register 15 along with a data value that indicates whether the sensor 14 is functioning correctly. The operation of the input node 18 and the output node 16 are discussed in more detail above with reference to Figures 2 and 3.

Those of ordinary skill in the art will recognize that power input node 22 and the clock input node 24 can also be coupled to a common clock node and power node within the integrated circuit 12 should a baseline temperature measurement with all operating elements in an off state not be necessary. The ground node 20 typically shares a common ground plane with the exemplary integrated circuit 12. Moreover, those skilled in the art will recognize that the input node 18 and the output node 16 can be adapted to provide the sensor 14 with an interface internal to the exemplary integrated circuit 12.

Figure 2 is a waveform diagram that illustrates the digital signals communicated to the input node 18 and from the output node 16. The input signal 30 acts as a reset signal to reset the sensor 14 and initiate a sensing operation by the sensor 14. The output signal 32 is a digital signal that toggles between a logic "0" level and a logic "1" level to communicate the first value, the second value and the third value of the sensor 14 in serial fashion. Figure 3 illustrates the steps taken by the sensor 14 to report a sensed physical stimulus. Upon power up of the sensor 14, the state of the sensor is unknown. As such, the input signal 30 is held asserted to a logic level "0" at the input node 18 to force the sensor 14 to its initial or starting state. By forcing the sensor 14 to its starting state the content of the register 15 is reset. The sensor 14 remains in this state until the input signal 30 asserted at the input node 18 rises to a logic "1" level following at least one clock cycle of the clock signal asserted on the clock input node 24. Those skilled in the art will recognize that sensor 14 can be configured so that when the input signal 30 is asserted to a logic "1" level at the input node 18 to force the sensor 14 to its initial or starting state. Moreover, those skilled in the art will recognize that the input signal 30 can be asserted to a logic "0"

level at any time after the power on reset to again force the sensor 14 to its initial or starting state.

Once the input signal 30 rises to a logic "1" level on the input node 18, the sensor 14 initiates sensing a physical stimulus within the exemplary integrated circuit 12 to obtain an absolute or relative quantitative measurement (step 52 in Figure 3). During the sensing process of the sensor 14, the input signal 30 at the input node 18 is held at a logic "1" level and the output signal 32 asserted on the output node 16 is also held at a logic "1" level (step 52 in Figure 3). The logic "1" level of the output signal 32 asserted on the output node 16 indicates that the sensor 14 is obtaining a measurement of a physical stimulus, such as the internal temperature of the exemplary integrated circuit 12. Those skilled in the art will recognize that the sensor 14 can be configured so as the output signal 32 asserts a logic "0" level on the output node 16 to indicate that the sensor 14 is obtaining a measurement of a physical stimulus, such as the internal temperature of the exemplary integrated circuit 12. After a fixed number of clock cycles on the clock input node 24, the sensor 14 places a measurement value of the physical stimulus into the register 15 and deasserts the output signal 32 on the output node 16 for at least one clock cycle on the clock node 24 (step 54 in Figure 3).

After one clock cycle on the clock input node 24, the sensor 14 shifts the measured value of the physical stimulus out of the register 15 on the output node 16 at a rate of one bit per clock cycle on the clock input node 24 (step 56 in Figure 3). When the sensor has emptied the register 15, the sensor 14 affixes a second data value to the response and asserts the second data value on the output node 16 at the rate of

one bit per clock cycle on the clock input node 24 (step 58 in Figure 3). The second data value provides an indication that the sensor 14 is functioning correctly. As the output signal 32 illustrates, the affixed value corresponds to a 010 bit pattern. Nevertheless, those skilled in the art will recognize that the sensor 14 can affix an alternative bit pattern, such as 101 and the affixed value asserted by the sensor 14 can precede or follow the assertion of the measured value shifted out of the register 15. Moreover, those skilled in the art will recognize that the bit length of the measured response can vary depending on the application, the accuracy required and the like.

While the present invention has been described with referenced to a preferred embodiment thereof, one skilled in the art will appreciate various changes in form and detail may be made without departing from the intended scope of the present invention as defined in the pending claims. The logic "0" levels refer to throughout this text refer to a voltage level that is approximately 0 volts and the "1" levels referred to throughout this text refer to a voltage level that is at least approximately 1.0 volts.